Monolithic *RC* All-Pass Networks with Constant-Phase-Difference Outputs

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Abstract — **All-pass network techniques have made it possible to realize very small monolithic lumped active phase shifters with decade bandwidths, high yield, and relative phase stability, even when the device parameters vary ±20 percent. We have successfully demonstrated fully monolithic first-order networks (at 250 MHz) and second-order networks (at 4 GHz).**

I. Introduction

MICROWAVE phased-array systems traditionally have been designed with a binary set of phase shifters using distributed components. Unfortunately, applying those techniques to monolithic integrated circuits results in comparatively large chip size for frequencies below about 6 GHz. This problem has caused a strong interest in using lumped circuit techniques that enable chip size to be reduced drastically. Yet lumped phase shifters that depend on precise absolute values of device parameters often have low yield. This paper reports on a monolithic phase shifter implementation consisting of a pair of segmented modulators [1], [2] driven by pairs of signals derived from constant-phase-difference networks.

These constant-phase-difference networks are a monolithic version of a circuit first proposed by R. B. Dome in 1946 for generating single sideband modulation with audio frequencies [3]. The circuit consists of pairs of all-pass networks with only capacitors, resistors, and active elements. The poles and zeros of the transmission function lie on the real axis of the complex frequency plane, and the number of such pole and zero pairs determines the relative bandwidth over which the network will function with a small phase error. A first-order network with a single pole–zero pair is useful for narrow-band applications, while a second-order network can maintain a constant phase difference of 90° over a relative bandwidth of as much as 10 to 1, depending on the allowable errors in phase tracking.

An interesting property of the circuit is that the phase differences between the multiple outputs are primarily dependent on the ratio of resistor or capacitor values. This characteristic is ideal for monolithic technology, where the ratio of parameters is accurately determined by topological mask design, while the absolute values are a function of doping levels and deposition rates.

In addition, the magnitude of the needed capacitance decreases with increasing frequency. To implement the all-pass networks at 5 GHz, for example, capacitance values well under 1 pF are needed. In fact, only in a monolithic circuit are the unavoidable stray capacitances sufficiently small in comparison to make the circuit feasible.

The following sections of this paper report the design, fabrication, and evaluation of a first-order network intended for the 220–280-MHz frequency range and a second-order implementation for the 3–5-GHz range. Both networks were designed to generate four output signals having relative phases of 0°, 90°, 180°, and 270°. Digitally controlled on-chip RF switches allow the selection of four pairs of output signals, i.e., 0° and 90°; 90° and 180°; 180° and 270°; 270° and 0°. When either of the resulting vector generators is cascaded with the previously reported sine/cosine scalar element [1], [2], the result is a complete 0°–360° 5-bit phase shifter.

II. Theoretical Considerations

The four resistors and four capacitors shown within the outlined region in Fig. 1 constitute a basic first-order all-pass network, in which the relative *RC* time constants are designed in a manner to generate the required four signals which are 90° apart from one another in phase. The four signals are switched to the two output ports with digitally controlled GaAs FET RF switches. The all-pass network must be driven by two balanced, complementary RF signal sources of relatively low impedance. GaAs FET source followers are used to provide the low-impedance sources. The symmetry of the configuration ensures that these input source followers are loaded by equal impedances. The frequency dependence of this finite load impedance will result in a slightly frequency dependent amplitude response in all four output channels equally without affecting the relative phase and amplitude relationships among the channels.

The mode of operation for this type of network can be explained with the help of the voltage vector diagram of Fig. 2. The amplitude of the output vector is independent of frequency. When the two networks are designed properly, one network has a phase shift of 45° and the other a shift of 135° at the center of the operating frequency band.

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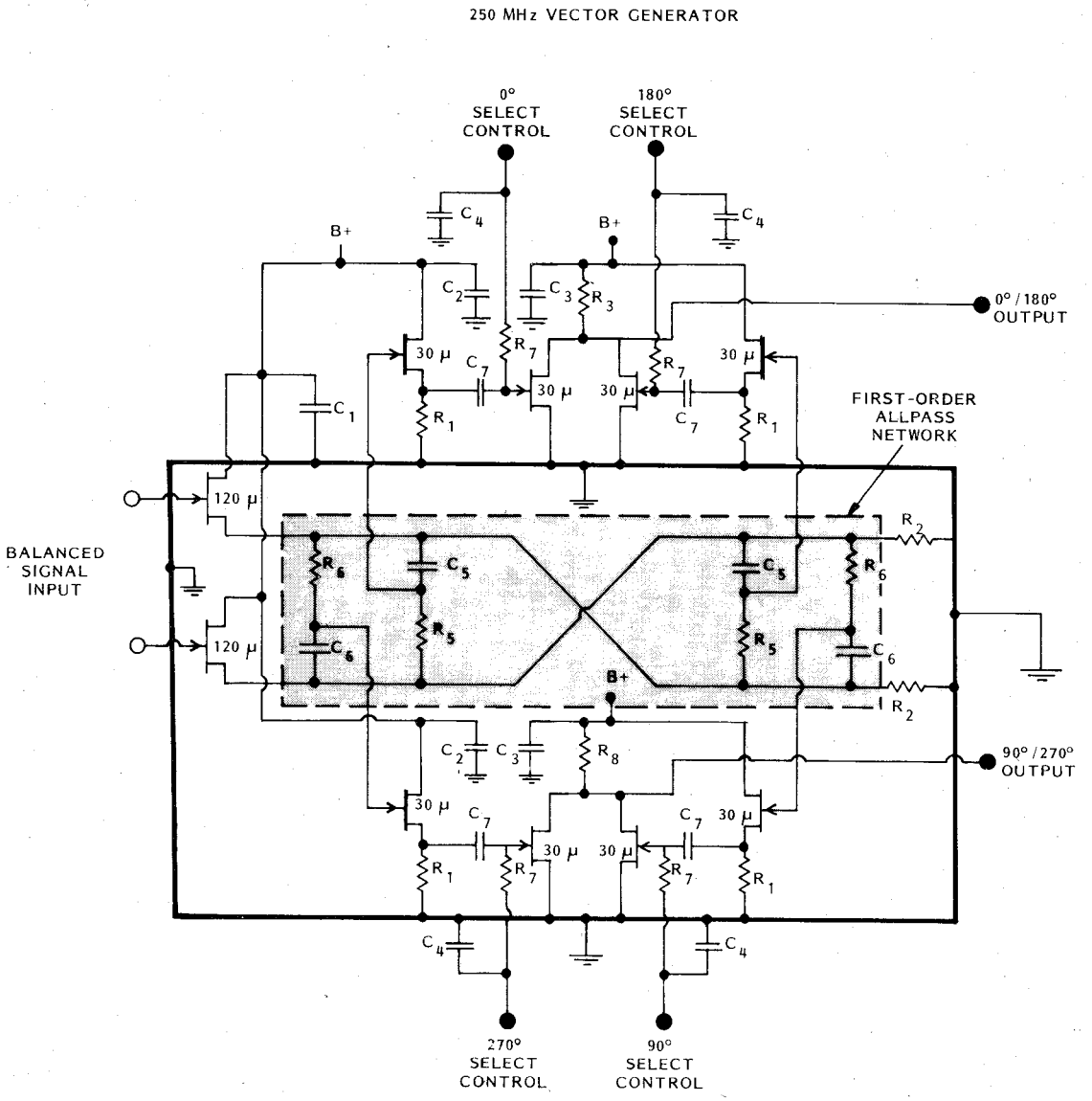

Fig. 1. Circuit schematic of the 250-MHz vector generator.

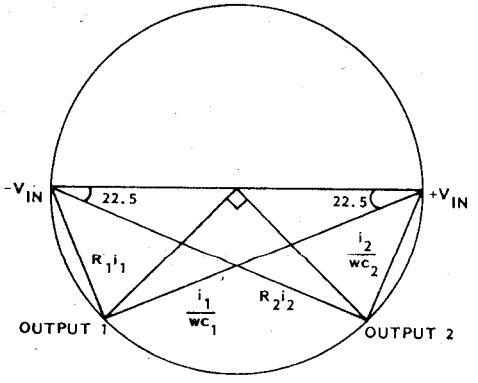

Fig. 2. Voltage vector diagram of a pair of all-pass networks.

A circuit configuration using a first-order network shows a phase response with a single peak. By selecting the element values so that the phase difference between the two branches exceeds the desired value of 90° by a small amount at the center, the circuit will operate over a certain band of frequencies without the phase error exceeding this amount. For example, for a 1° error at the center, the circuit will cover a 1.7 bandwidth ratio.

A second-order network can be created by cascading two first-order networks or by replacing the network shown in Fig. 1 with the one shown in Fig. 3. The resistor and capacitor network within the outlined region in Fig. 3 constitutes the second-order all-pass network. One disadvantage of the single-stage second-order network in comparison to a cascade of two first-order networks is its greater insertion loss. On the other hand, its apparent greater complexity is of little concern in a monolithic realization, since the small resistors and capacitors consume very little room on the substrate.

The theory for computing the location of the poles and zeros of the transfer function has been described in previous papers [3]–[5]. D. Weaver, in particular, shows a systematic numerical approach for deriving their locations [5]. For applications in which second-order networks satisfy the bandwidth requirements, simpler, more direct iterative computer programs can be used, since a second-order

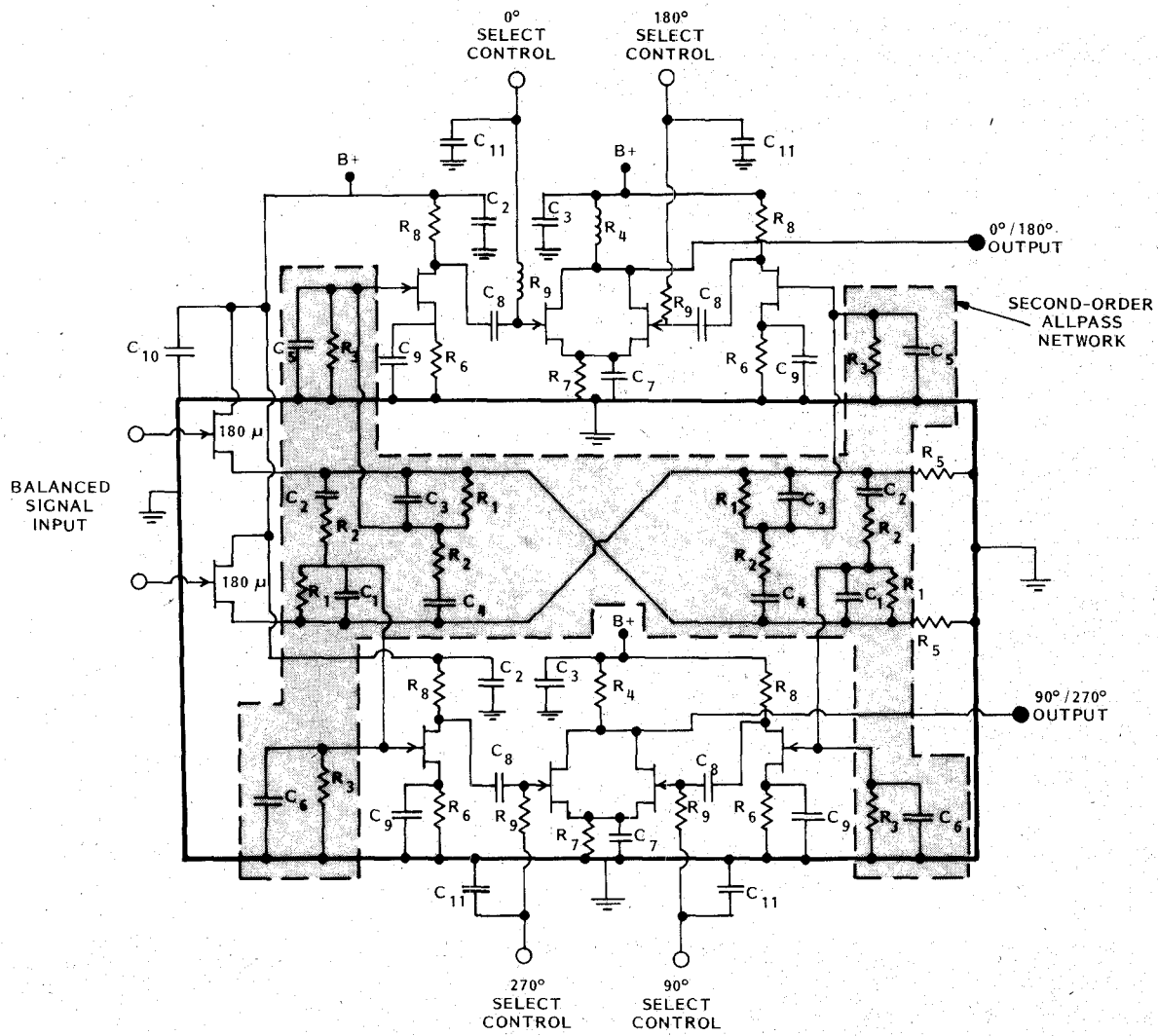

Fig. 3. Circuit schematic of the second-order vector generator (3–5 GHz).

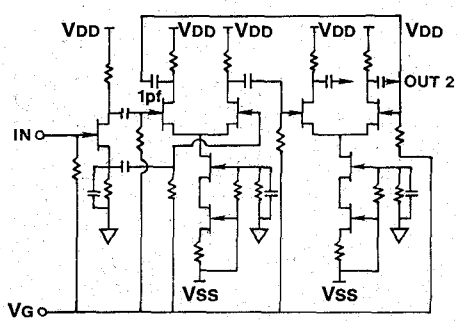

Fig. 4. Phase splitter.

network has only two independent numerical values that must be selected. These independent values are, first, the ratio between the pole locations of both networks and, second, the ratio of the center frequencies of the two networks.

III. The Phase Splitter

The phase splitter that generates the two out-of-phase signals, shown in Fig. 4, consists of an initial approximate phase splitter followed by differential pairs that have more gain for the odd mode than for the even mode. Since the even-mode component represents the deviation from a perfect split, the quality of the signal improves with each stage of differential gain. The initial split load resistor phase splitter gives a less than perfect split as a result of the presence of a finite gate current. However, the capacitive component of this gate current is partially compensated for by the small capacitor shunting the source load resistance.

IV. Circuit Implementations

Fig. 5 presents a photograph of the VG-2 cell, which is an implementation of the first-order circuit shown in Fig. 1. It was designed for operation at a center frequency of 250 MHz. The cell was fabricated using an epitaxial GaAs process with air-bridge crossovers, metal–insulator–metal (MIM) capacitors, bulk GaAs resistors, and 1-μm-gate-length MESFET active devices. The chip size is 1.2× 1.2 mm. Fig. 6 shows the RF performance over the 180–340-MHz band, measured at wafer level on a coplanar RF probe station.

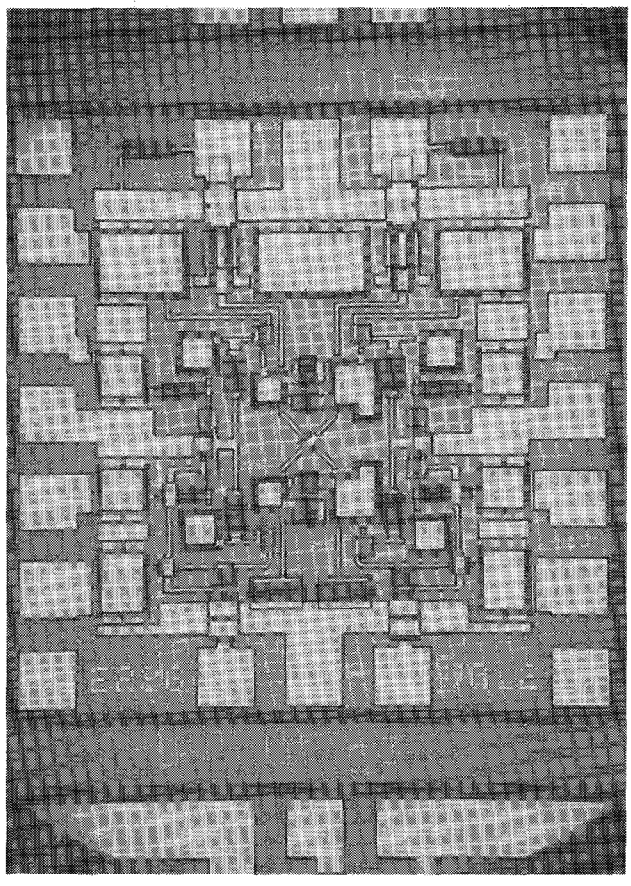

Fig. 5. Photograph of a vector generator at 250 MHz.

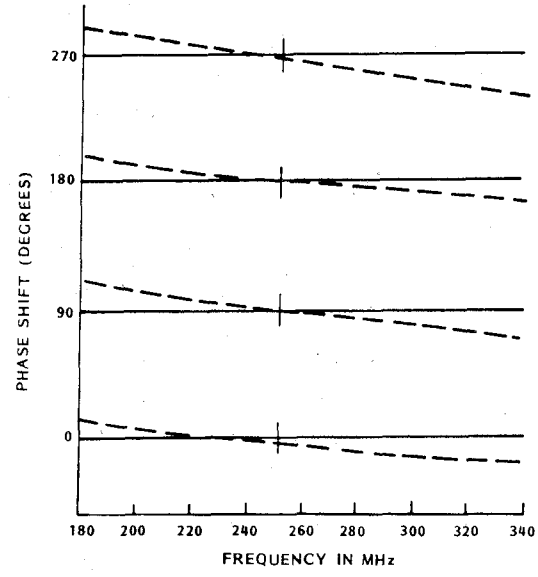

Fig. 6. RF performance of the 250-MHz vector generator.

Fig. 7 shows a VG-3 second-order constant-phase-difference network, which is shown schematically in Fig. 3. It is combined on the same chip with a PSP-1 phase splitter, shown in Fig. 4. The composite device was fabricated with a selectively ion implanted process with air-bridge crossovers, MIM capacitors, thin-film resistors, and 1-μm-gate-length MESFET active devices. The chip size is 1.2×2.4 mm. Fig. 8 presents the experimental results of wafer-level

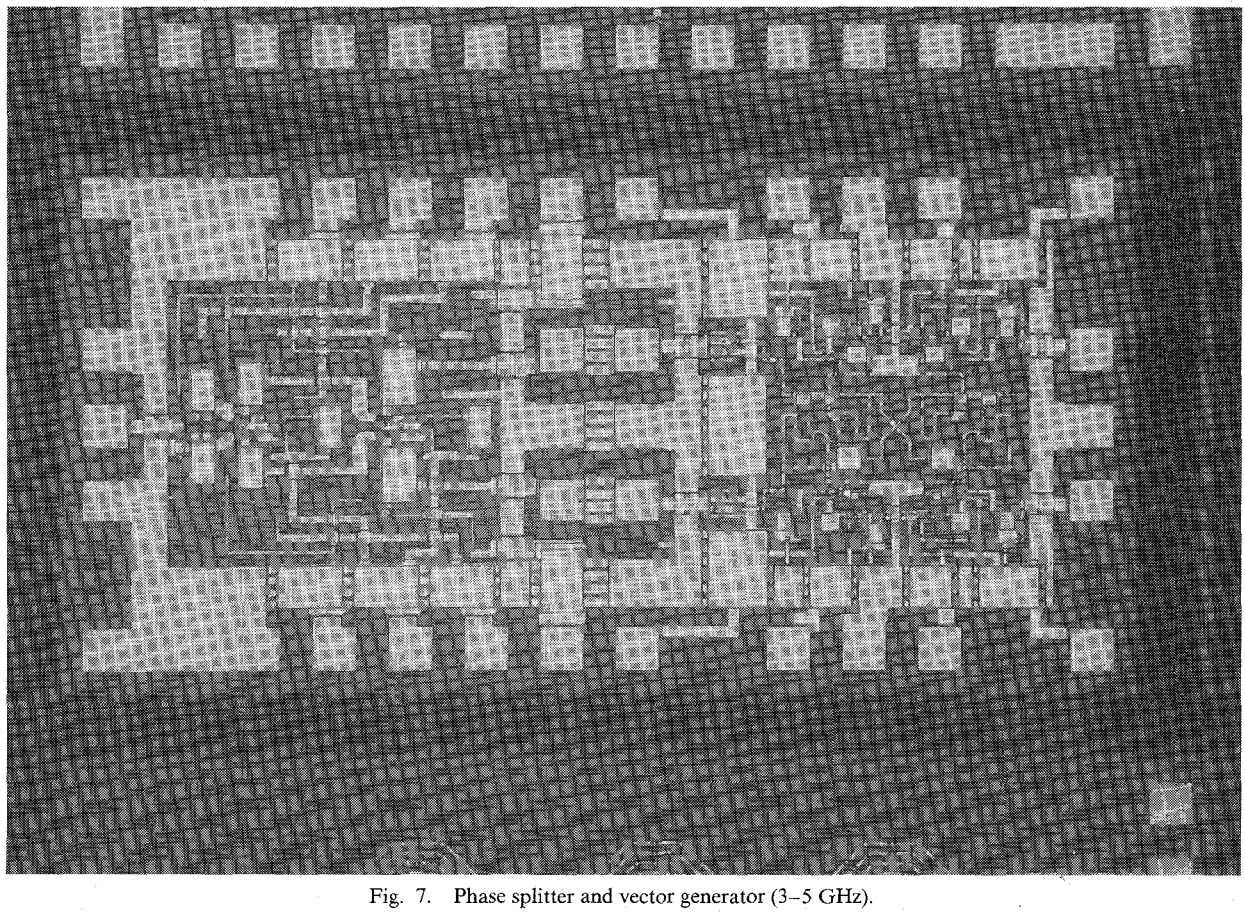

Fig. 7. Phase splitter and vector generator (3–5 GHz).

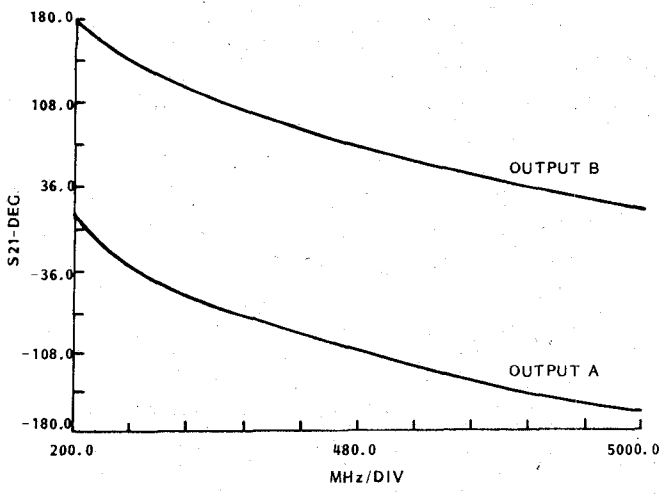

Fig. 8. Wafer-level RF test results for differential phase splitter circuit PSP-1.

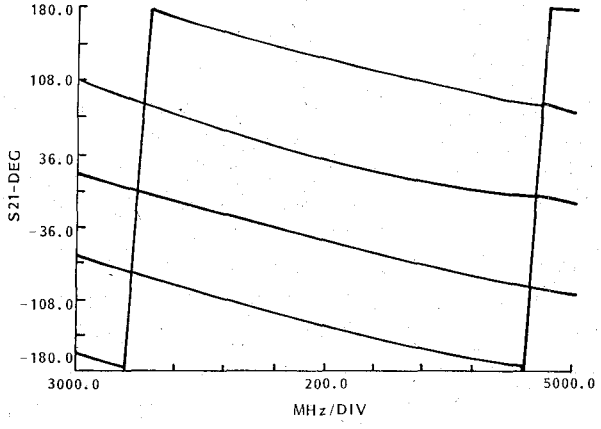

Fig. 9. Composite results of both cells over 3–5 GHz.

RF testing for only the phase splitter portion of the circuit (the left half of Fig. 7). The phase splitter demonstrated excellent performance over the 200-MHz-to-5-GHz frequency range: ± 0.25 dB amplitude match between the two outputs and the phase difference within 1.2° of the ideal 180°. Fig. 9 shows the composite response of both cells of Fig. 7 over the 3–5-GHz range.

V. Conclusions

Monolithic circuits based on *RC* all-pass networks are a viable means of implementing signal generators with constant-phase-difference outputs. Such signal generators can be fabricated using a very small chip area even at lower microwave frequencies, and they can be used to create monolithic active phase shifters by combining them with modulators. The balanced signals needed to drive the balanced all-pass networks can be monolithically implemented using a differential amplifier technique.

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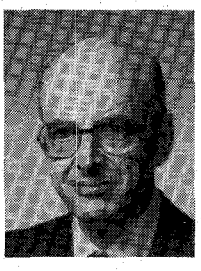

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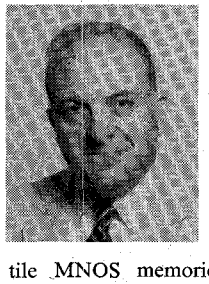

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